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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/781,477	02/17/2004	Juan I. Martinez	200314423-1	3109

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HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
RIAD, AMINE	
ART UNIT	**PAPER NUMBER**
2113	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/781,477	MARTINEZ ET AL.	
	Examiner	Art Unit	
	Amine Riad	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/01/06*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed action

Claims 1-30 have been presented for examination.

Claims 1-30 have been rejected

Objection

Claim 21 recites " The system of claim 21", it appears that claim 21 depends from claim 20. Correction is highly suggested.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Murthy US Patent 6,732,298.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in

the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

In regard to claim 1,

Murthy discloses a method of reboot reporting comprising:

- Reading a plurality of input lines associated with a plurality of computer systems having a plurality of processors;(Figure 1; items 10A,10B,10C,10D)
- Generating at least one non-maskable interrupt signal; (Column 2; lines 61-62)
- Outputting the non-maskable interrupt signal to a processor of the plurality of computer systems; (Column 2; lines 63-64) [When the nonmaskable pseudo interrupt **informs** it is being outputted to the processor]
- Outputting the non-maskable interrupt signal to a manager associated with the plurality of computer systems; (Column 4; lines 18-21) [Murthy disclose "that if it is desired for the computer system to have a dedicated display device ...a video graphic controller would interface the display device to the system. The display may comprise any suitable electronic display device upon which any image or text can be represented." Examiner considers the display as a mean for outputting the non-maskable interrupt to a manager because a manager needs a display terminal to receive this outputs]

- Generating an indication that at least one computer system has a fault condition. (Column 2; lines 63-65) [Examiner considers informing the processor that the array controller board is inoperative as an indication of a fault]

In regard to claim 2,

Murthy discloses the method of claim 1 further comprising associating the non-maskable interrupt signal with at least one computer system of the plurality of computer systems.(Figure1; items 50A,50B,50C) [this is where the NMI happens]

In regard to claim 3,

Murthy discloses the method of claim 2 further comprising generating a notice identifying the at least one computer system.(Column 6; lines 46-52) [debugging with the NMI means first that the item to be debugged is identified before starting the debugging.]

In regard to claim 4,

Murthy discloses the method of claim 3 further comprising redistributing the processing load from the at least one computer system to the remaining plurality of computer systems. (Column 8; lines 17-21) [because the remainder of system 100 is not effected it means that the system has a redistribution system in case a fault happens in one of its elements.]

In regard to claim 5,

Murthy discloses the method of claim 1 further comprising counting the number of times the non-maskable interrupt signal is generated. (Column 4; lines 36-39) [Examiner considers the LPC as a pin that counts the NMIs]

In regard to claim 6,

Murthy discloses a system for reboot reporting comprising:

- a plurality of computer systems having at least one processor and at least one non-maskable interrupt output;(Figure 1; items 50A,50B,50C) and (Figure 2; item 50) and (Column 2; lines 63-65)
- a manager system in circuit communication with the plurality of computer systems and comprising at least one non-maskable interrupt input associated with the plurality of computer systems. (Column 4; lines 18-21) [Murthy disclose "that if it is desired for the computer system to have a dedicated display device ...a video graphic controller would interface the display device to the system. The display may comprise any suitable electronic display device upon which any image or text can be represented." Examiner considers the display as a mean for outputting the non-maskable interrupt to a manager because a manager needs a display terminal to receive this outputs]

In regard to claim 7,

Murthy discloses the system of claim 6 wherein the plurality of computer systems comprises a plurality of non-maskable interrupt outputs (Figure 1; items 50A,50B,

50C) [each controller can generate an interrupt] and the manager system comprises a plurality of non-maskable interrupt inputs (Column 4; line 26) [Examiner considers when any image or text can be dislayed that means that the manger receives plurality of NMI].

In regard to claim 8,

Murthy discloses the system of claim 7 wherein the non-maskable interrupt outputs of the plurality of computer systems are in circuit communication with the plurality of non-maskable inputs of the manager system. (Figure 1; item 20) [PCI couples item 50 to item 22 and item 28 where it is possible to locate the display considered as manger as demonstrated before].

In regard to claim 9,

Murthy discloses the system of claim 6 wherein the plurality of computer systems comprises

- least one computer system having a processor, (Figure 1; item 10)
- a first bridge circuit (Figure 2; item 54)
- second bridge circuit and wherein the second bridge circuit comprising a non-maskable interrupt signal output in circuit communication with the processor (Figure 2; item 64).

In regard to claim 10,

Murthy discloses the system of claim 9 wherein the non-maskable interrupt output of the second bridge is in circuit communication with the manager system. (Figure 2) [Figure shows that item 64 is coupled to item 54 through PCI 56 which in turn is connected to the rest of the system with PCI 20, PCI 20 is coupled to LPC24, and ends item 28 where it is possible to locate the display considered as manger as demonstrated before].

In regard to claim 11,

Murthy discloses the system of claim 6 further comprising logic for reading at least one non-maskable interrupt input associated with the plurality of computer systems.(Column 3; lines 5-8)

In regard to claim 12,

Murthy disclose the system of claim 11 further comprising logic for generating an indication that at least one computer system has a fault condition based on the presence of a non-maskable interrupt signal present on the at least one non-maskable interrupt input. (Column 3; lines 9-10)

In regard to claim 13,

Murthy discloses a system for reboot reporting comprising:

- a plurality of computers comprising at least one means for processing; (Figure 1; item 10)

- means for managing the plurality of computers;(Column 3; lines 66-67) and (Column 4; lines 1-6)

- and means for outputting a non-maskable interrupt signal indicating a fault condition associated with at least one of the plurality of computers to the means for managing. (Column 2; lines 63-64) [When the nonmaskable pseudo interrupt **informs** it is being outputted to the processor]

In regard to claim 14

Murthy discloses the system of claim 13 further comprising means for detecting the non-maskable interrupt signal indicating a fault condition associated with at least one of the plurality of computers and generating a detection signal in response thereto. (Column 3; lines 9-10)

In regard to claim 15,

Murthy discloses the system of claim 13 further comprising means for generating at least one non-maskable interrupt signal. (Column 2; lines 61-62)

In regard to claim 16,

Murthy discloses the system of claim 13 further comprising means for generating an indication that at least one computer has a fault condition. (Column 2; lines 63-65) [Examiner considers informing the processor that the array controller board is inoperative as an indication of a fault]

In regard to claim 17,

Murthy discloses the system of claim 13 further comprising means for associating the non-maskable interrupt signal with at least one computer of the plurality of computers. (Figure1; items 50A, 50B, 50C) [This is where the NMI happens]

In regard to claim 18,

Murthy discloses the system of claim 17 further comprising means for redistributing the processing load from the at least one computer to the remaining plurality of computers. (Column 8; lines 17-21) [Because the remainder of system 100 is not effected it means that the system has a redistribution system in case a fault happens in one of its elements.]

In regard to claim 19,

Murthy discloses the method of claim 13 further comprising means for counting the number of times the non-maskable interrupt signal is generated. (Column 4; lines 36-39) [Examiner considers the LPC as a pin that counts the NMIs]

In regard to claim 20,

Murthy discloses a computer system comprising:

- a processor; (Figure 2; item 58)
- a memory; (Figure 2; items 60 & 50)

- at least one bridge circuit in circuit communication with the processor;(Figure 2; item 64)

- a non-maskable interrupt signal circuit in circuit communication with the processor and at least one other computer system.(Figure 2;item 59)

In regard to claim 21,

Murthy discloses the system of claim 21 wherein the at least one other computer system comprises an enclosure manager. (Column 4; lines 18-21) [Murthy discloses "that if it is desired for the computer system to have a dedicated display device ...a video graphic controller would interface the display device to the system. The display may comprise any suitable electronic display device upon which any image or text can be represented." Examiner considers the display as a mean for outputting the non-maskable interrupt to a manager because a manager needs a display terminal to receive this outputs and it is enclosed]

In regard to claim 22,

Murthy disclose system comprising:

- an enclosure having a plurality of individual computer systems and a manager computer system;(Column 3; line 56) [A server is an enclosure]

- wherein at least one of the plurality of computer systems comprises a processor and a non-maskable interrupt signal circuit, the non-maskable interrupt signal

circuit in communication with the processor and the manager computer system,(Figure 2; items 58,59 and PCI 56 and 20 and item 28 of figure 1)

- the non-maskable interrupt signal circuit comprising a bridge circuit and a non-maskable interrupt signal path to the processor and the manager computer system. (Figure 2; item 64; and PCI 56 and 20)

In regard to claim 23,

Murthy discloses the system of claim 22 wherein the manager computer system comprises a non-maskable interrupt signal input. (Column 4; lines 25-26) [Because the display manager contains a text that will display an NMI message, his message has to come from an input]

In regard to claim 24,

Murthy discloses the system of claim 23 wherein the manager computer system comprises logic for reading a state of the non-maskable interrupt signal input. (Column 3; lines 5-8)

In regard to claim 25,

Murthy discloses the system of claim 24 wherein the manager computer system comprises logic for generating a notice based on the state of the of the read non-maskable interrupt signal input. (Column 4; line 26) [the text message is considered as a notice]

In regard to claim 26,

Murthy discloses a system comprising:

- Means for housing a plurality of digital devices; (Figure 1; item 100)
- Means for managing the plurality of digital devices,(Column 3 and 4; lines 66-67, lines 1-5)
- Means for managing comprising a location within said means for housing;(Figure 1; item 28)
- Means for receiving and processing executable instructions,(Figure 2; item 58)
- Means for receiving and processing comprising a location within said means for housing; (Figure 1; item 22)
- Means for generating a non-maskable interrupt signal; (Figure 2; item 50)
- Means for communicating the non-maskable interrupt signal to the means for receiving and processing and to the means for managing. (Figure 2; items 56 & 20)

In regard to claim 27,

Murthy discloses the system of claim 26 wherein the means for communicating the non-maskable interrupt signal to the means for receiving and processing and to the means

for managing comprising a non-maskable interrupt signal pathway. (Figure 2; items 56 & 20)

In regard to claim 28,

Murthy discloses the system of claim 26 wherein the means for managing the plurality of digital devices comprises means for reading the state of the means for communicating and means for generating a notice based on the state of the means for communicating. (Column 3; line 8) and (Figure 2; item 64)

In regard to claim 29,

Murthy discloses the system of claim 26 wherein the means for managing the plurality of digital devices comprises means for redistributing a processing distribution among the plurality of digital devices. (Column 8; lines 17-21) [because the remainder of system 100 is not effected it means that the system has a redistribution system in case a fault happens in one of its elements.]

In regard to claim 30,

Murthy discloses the system of claim 26 wherein

the means for generating a non-maskable interrupt signal comprises a bridge circuit associated with the means for receiving and processing. (Figure 2; item 64) and (Figure 1; item 22 and 28)

Response to Applicant's Argument

Applicant arguments filed on December 1, 2006 have been fully considered, and are not persuasive.

In regard to the first argument in which the Applicant states that "It is respectfully submitted that Murthy fails to disclose the use of a non-maskable interrupt in any form"

Examiner respectfully disagrees, and points out that Murthy discloses in the summary of the invention that " The problems noted above are solved in large part by a single level interrupt processor on the array controller board that contains a critical failure input line that permits implementation of non-maskable pseudo-interrupt for debugging of the array controller." Murthy adds "the non-maskable pseudo-interrupt informs the processor of a debug request even when all device interrupts in the processor are disabled"

Murthy's summary proves that Murthy uses a non-maskable interrupt.

In regard to the second argument in which the Applicant states, "It is respectfully submitted that Murthy fails to teach or disclose that non maskable interrupts are used with a processor and a manager" Examiner respectfully disagrees.

Applicant is reminded that the application defines a manager *as any programmed or programmable device that can store, retrieve, and process data for exercising executive administrative, and supervisory direction, or control of other electronic devices.* Examiner guides Applicant to Figure 1, which shows elements 10A, 10B, 10C, and 10D, coupled to element 22 an Input/Output controller Hub that is in turn connected to

element 28 Super I/O controller. According to Applicant's definition of a manager, Examiner considers the combination of elements 22 and 28 as a manager because Murthy discloses "The super Input/Output controller 28 also couples to the ICH 22 via LPC bus 24 and controls various system functions including interfacing with various input and output devices such as keyboard 30. The super I/O controller 28 may further interface, for example, with a system pointing device such as a mouse 32, various serial ports" It is clear that the combination of elements 22 and 28 gets executive supervisory direction from items 32 and 30, and consequently makes Applicant argument not valid.

In regard to the third argument in which the Applicant states that "It is respectfully submitted that nowhere does this disclosure [If it is desired for the computer system to have a dedicated display device, such a system could be implemented by coupling a video adapter card to the host bridge 14 by was of expansion bus 18 or a separate bus] teach, much less suggest, "outputting the non maskable interrupt signal to a manager associated with the plurality of computer systems, " as claimed" Examiner respectfully disagrees, and points Applicant to the previous argument answer, where Examiner elaborates how the combination of items 28, 30 28, and 22 is considered as means for managing and outputting non-maskable interrupts.

In regard to the fourth argument in which the Applicant states, "Additionally, claim 20 requires the non-maskable interrupt signal circuit to be in communication with the processor and at least one other computer system. Murthy's Figure 2 shows interrupt line as only being output to processor 58 and not to other computer system" Examiner respectfully disagrees. Figure 2 couples processor 58 to a processor bridge 64 by link

59, the processor bridge in turn is coupled to test equipment which the Examiner considers as another computer system. This proves that Applicant argument is not valid.

In regard to claim 5 argument, which states that "Applicant cannot find any support for such teaching" Examiner respectfully disagrees. Examiner points Applicant to (Column 6; lines 21-25) where Murthy discloses "As shown in figure 2, various interrupts (int0 int1, int2...) are generated by the devices given in figure 1 and figure 2, and handled by processor 58" Examiner considers the listing of int0, int1, int2, as counting interrupts.

The response above proves that Applicant's arguments are not valid.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Amine Riad whose telephone number is 571-272-8185. The examiner can normally be reached on 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on 571-272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

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AR
Amine Riad
Patent Examiner
2/5/2006

ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100